This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A semiconductor field-effect transistor device comprising:

a first strained layer of semiconductor material doped of a first dopant type formed on a substrate;

a source region and a drain region implanted with dopants of a second opposite type;

a gate electrode separated from the first layer by a dielectric region, and positioned between said source and drain regions;

said substrate having one or more threading dislocations, misfit dislocations or crystal defects that extend continuously from the source region to the drain region at an interface between said first strained layer of semiconductor material and said substrate, and

blocking impurity dopant materials selected from the group comprising: In, Pb, Sb and Sn, that partially or fully occupies each said one or more threading dislocations, misfit dislocations or crystal defects along said interface, wherein said blocking impurity dopant materials substantially inhibit diffusion of said implanted source and drain dopants from diffusing along said threading dislocations, misfit dislocations or crystal defect along said interface.

2. (Original) The semiconductor field-effect transistor device as claimed in Claim 1, wherein said first layer of semiconductor material comprises material selected from the group comprising: Si, SiGe, SiGeC, or Ge.

3. (Canceled)

4. (Previously Presented) The semiconductor field-effect transistor device as claimed in Claim 1, wherein said substrate comprises a SiGe relaxed substrate.

5. (Original) The semiconductor field-effect transistor device as claimed in Claim 1, wherein said source and drain dopants of said second type comprise P, As or Sb, singly or in combination thereof, and said blocking impurity is In.

6. (Original) The semiconductor field-effect transistor device as claimed in Claim 1, wherein said source and drain dopants of said second type comprise B or In, singly or in combination thereof, and said blocking impurity is Sb.

7. (Original) The semiconductor field-effect transistor device as claimed in Claim 1, wherein said blocking impurity is a neutral-type impurity.

8. (Original) The semiconductor field-effect transistor device as claimed in Claim 7, wherein said blocking impurity is a group IV impurity.

9. (Currently Amended) The semiconductor field-effect transistor device as claimed in Claim 7, wherein said blocking impurity [[is]] dopant comprises C, ~~Sn or Pb,~~ singly or in combination with said Sn or Pb ~~thereof~~.

10. (Withdrawn) A method for forming a semiconductor field-effect transistor device comprising the steps of:

a) forming a first semiconductor structure comprising material doped of a first dopant type such that said semiconductor structure includes a non-zero number of threading dislocations;

b) implanting a blocking impurity in said semiconductor structure;

c) thermally processing said semiconductor structure such that said blocking impurities segregate to said existing threading dislocations, said blocking impurities further segregating to new dislocations that may be induced by said thermal processing;

d) forming a dielectric layer on top of said semiconductor structure to define a gate region, and forming a gate electrode over said dielectric region, a portion of the semiconductor structure immediately beneath the gate defining a channel region, and a portion of the semiconductor structure beneath the channel region defining a well region; and,

e) implanting dopants in said semiconductor structure on opposite sides of said gate region to form source and drain regions such that the source and drain regions abut the channel region and well region on either side,

wherein a dislocation or crystal defect extends continuously from said source to drain region, and an immediate vicinity of said crystal defect is substantially occupied by said blocking impurity dopant.

11. (Withdrawn) The method for forming a semiconductor field-effect transistor device as claimed in Claim 10, wherein said first layer of semiconductor material comprises material selected from the group comprising: Si, SiGe, SiGeC, or Ge.

12. (Withdrawn) The method for forming a semiconductor field-effect transistor device as claimed in Claim 10, wherein said step a) of forming a first semiconductor structure

comprises forming a multi-layer structure comprising materials selected from the group comprising: Si, SiGe, SiGeC, or Ge.

13. (Withdrawn) The method for forming a semiconductor field-effect transistor device as claimed in Claim 10, wherein said first semiconductor structure comprises a SiGe relaxed substrate.

14. (Withdrawn) The method for forming a semiconductor field-effect transistor device as claimed in Claim 10, wherein said step b) of implanting blocking impurity dopant materials in said semiconductor structure includes implanting a blocking impurity of a concentration ranging between about 10^{17} cm^{-3} - 10^{19} cm^{-3}.

15. (Withdrawn) The method for forming a semiconductor field-effect transistor device as claimed in Claim 10, wherein said step b) of implanting blocking impurity dopant materials in said semiconductor structure includes implanting a blocking impurity with an energy such that the peak blocking impurity concentration approximately coincides with a Si/SiGe interface.

16. (Withdrawn) The method for forming a semiconductor field-effect transistor device as claimed in Claim 10, wherein said thermally processing step c) comprises a thermal annealing step at an anneal temperature ranging between about 600 °C – 1200 °C.

17. (Withdrawn) The method for forming a semiconductor field-effect transistor device as claimed in Claim 10, wherein dopants forming said source and drain regions comprise P, As or Sb, singly or in combination thereof, and said blocking impurity is In.

18. (Withdrawn) The method for forming a semiconductor field-effect transistor device as claimed in Claim 10, wherein dopants forming said source and drain regions comprise B or In, singly or in combination thereof, and said blocking impurity is Sb.

19. (Withdrawn) The method for forming a semiconductor field-effect transistor device as claimed in Claim 10, wherein said blocking impurity is a neutral-type impurity.

20. (Withdrawn) The method for forming a semiconductor field-effect transistor device as claimed in Claim 18, wherein said blocking impurity is a group IV impurity.

21. (Withdrawn) The method for forming a semiconductor field-effect transistor device as claimed in Claim 18, wherein said blocking impurity is C, Sn or Pb, singly or in combination thereof.